Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An encoder for encoding a~~-~~digital signal transmitted as MPEG-2 transport stream (TS) packets over the Serial Data Transport Interface (SDTI), the encoder comprising:

a clock; and

a first means for deriving timing information relating to the digital signal from the clock, wherein the digital signal comprises:

data blocks, each data block including a header containing data relating to the block and a plurality of slots, each slot having a slot header relating to the slot and a data packet;

a plurality of data packets containing at least a first part and subsequent parts of the digital signal,

a first slot including said first part of the digital signal and a reference time defining a time of production of the first part, and

each subsequent slot containing a subsequent part of the digital signal and timing information defining a time of production of said subsequent part relative to the reference time;

said first means deriving from the clock, the reference time defining the time of production of said first part and said timing information defining the times of production of the subsequent parts,

wherein said first means is configured to provide the timing information of each data packet relative to other data packets in said plurality of data packets, and

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wherein a slot coarse count and a slot sub count in said plurality of slots transmitted over the MPEG-2 TS are used to generate the reference time.

2. (Original) An encoder according to claim 1, wherein the timing information comprises coarse and fine timing information.

3. (Original) An encoder according to claim 2, wherein the clock comprises an input for receiving a clock signal, a modulo n counter which counts the clock signal and divides the clock signal frequency by n to produce the fine time information and a modulo m counter which counts the frequency divided clock signal produced by the modulo n counter, to produce the coarse time information, wherein m is much greater than n.

4. (Original) An encoding according to claim 3, wherein the clock signal frequency is 2.25n Mhz, where n is an integer.

5. (Original) An encoder according to claim 4, wherein the clock signal frequency is 27MHz, n is 12 and m is 65536.

6. (Original) An encoder according to claim 4, wherein the clock signal frequency is 36MHz, n is 16 and m is 65536.

7. (Original) An encoder according to claim 1, comprising a multiplexer for inserting the time information in the slots.

8. (Previously Presented)   An encoder according to claim 1, further comprising means for inserting into the slot header a flag indicating whether the slot contains said first packet.

9. (Previously Presented)   An encoder according to claim 1, wherein the said data blocks are variable length blocks.

10. (Original) An encoder according to claim 9, wherein the said slots are variable length slots.

11. (Original) An encoder according to claim 10, wherein the variable length slots comprise slots containing metadata and slots containing data described by the metadata.

12. (Original) An encoder according to claim 11, wherein a metadata slot precedes the data slots containing the data described by the metadata in the metadata slot.

13. (Original) An encoder according to claim 12, wherein the metadata slot contains metadata identifying a succeeding slot which contains a said first packet.

14. (Original) An encoder according to claim 11, wherein the variable length slots comprise a data field, a Type field containing data describing the type of data in the Data field and a Length Field defining the length of the data in the data field.

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15. (Canceled)

16. (Currently Amended) A decoder for decoding a~~a~~ digital signal <u>transmitted as MPEG-2 transport stream (TS) packets over the Serial Data Transport Interface (SDTI), the digital signal</u> comprising data blocks, each data block including a header containing data relating to the block and a plurality of slots, each slot having a slot header relating to the slot and a data packet of a plurality of data packets, the plurality of data packets containing successive parts of information from a source, a first slot which contains a first packet containing a first part of the said information from the source also containing a reference time, and each subsequent slot containing a subsequent packet of the information from the said source also containing timing information defining the timing of that packet relative to the reference time, the decoder comprising:

a clock,

first means for detecting the timing information of the plurality of data packets,

second means for initially setting the clock to the said reference time on detection of said first packet,

third means for comparing the clock time with the said timing information of the subsequent packets,

fourth means for outputting the packets at the times when the timing information of the packets equals the clock time, and

fifth means for providing timing information of each data packet relative to other data packets in the plurality of data packets,

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wherein a slot coarse count and a slot sub count in said plurality of slots transmitted over the MPEG-2 TS are used to generate the reference time.

17. (Original) A decoder according to claim 16, wherein the timing information comprises coarse and fine timing information.

18. (Original) A decoder according to claim 17, wherein the clock comprises an input for receiving a clock signal, a modulo n counter which counts the clock signal and divides the clock signal frequency by n to produce the fine time information and a modulo m counter which counts the frequency divided clock signal produced by the modulo n counter, to produce the coarse time information, wherein m is much greater than n.

19. (Original) A decoder according to claim 18, wherein the clock frequency is 2.25MHz, wherein n is an integer.

20. (Original) A decoder according to claim 19, wherein the clock signal frequency is 27MHz, n is 12 and m is 65536.

21. (Previously Presented) A decoder according to claim 19, wherein the clock signal frequency is 36MHz, n is 16 and m is 65536.

22. (Original) A decoder according to claim 16, for use with a signal the slot header of which contains a flag indicating whether the slot contains a said first packet, the decoder

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comprising a demultiplexer for separating the flag and the packet, and means responsive to the

flag for setting the clock to the reference time if the flag indicates a first packet.

23. (Original) A decoder according to claim 16, wherein the outputting means comprises

a FIFO buffer.

24. (Canceled)

25. (Currently Amended) A digital signal transmitted as MPEG-2 transport stream (TS)

packets over the Serial Data Transport Interface (SDTI), the digital signal comprising:

data blocks, each data block including a header containing data relating to the block and

at least one slot ;

each slot having a slot header relating to the slot and a data packet of a plurality of data

packets; the plurality of data packets containing successive parts of information from a source;

a first slot which contains a first packet containing a first part of the said information

from the source also containing a reference time; and

each subsequent slot containing a subsequent packet of the information from the said

source also containing timing information defining the timing of that packet relative to the

reference time,

wherein each part of said information provides timing information of each data packet

relative to other data packets in said plurality of data packets, and

wherein a slot coarse count and a slot sub count in said plurality of slots transmitted over

the MPEG-2 TS are used to generate the reference time.

26. (Previously Presented) A signal according to claim 25, wherein the timing information of each data packet comprises coarse timing information and fine timing information.

27. (Original) A signal according to claim 26, wherein the coarse and fine timing information are represented by separate words in the slot header.

28. (Original) A signal according to claim 25, wherein the slot header includes data indicating whether or not the packet is a first packet.

29. (Original) A signal according to claim 25, wherein the slot header includes data indicating packet type.

30. (Original) A signal according to claim 29, wherein the data indicating packet type indicates one or both of (i) packet length; and (ii) whether the packet includes active error correction data.

31. (Original) A signal according to claim 30, wherein each packet includes error correction data.

32. (Original) A signal according to claim 31, wherein the slot header includes data indicating whether or not the slot contains error correction data.

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33. (Original)   A signal according to claim 32, wherein each slot contains error correction data.

34. (Original)   A signal according to claim 25, wherein the slots of each block are of fixed length and have predetermined positions in the block.

35. (Original)   A signal according to claim 25, wherein the said data blocks are variable length blocks.

36. (Original)   A signal according to claim 35, wherein the said slots are variable length slots.

37. (Original)   A signal according to claim 36, wherein the variable length slots comprise slots containing metadata and slots containing data described by the metadata.

38. (Original)   A signal according to claim 37, wherein a metadata slot precedes the data slots containing the data described by the metadata in the metadata slot.

39. (Original)   A signal according to claim 38, wherein the metadata slot contains metadata identifying a succeeding slot which contains a said first packet.

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40. (Original) A signal according to claim 36, wherein the variable length slots comprise a data field, a Type field containing data describing the type of data in the Data field and a Length Field defining the length of the data in the data field.

41. (Canceled)

42. (Original) A signal according to claim 35, wherein the said packets are MPEG 2 TS packets or ATM cells or Internet Protocol Packets.

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